Soft Switching Interleaved High Step-Up Converter With Multifunction Coupled Inductors

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***Abstract*—This article presents an efficient interleaved soft switching dc–dc converter for high step-up applications. In the proposed converter, two multifunction coupled inductors are employed to increase the voltage gain, accomplish soft switching operation for all semiconductors in a wide range of load variations, and smooth the input current. Besides, the leakage inductance energy is recovered to enhance the voltage gain and efficiency while assisting soft switching condition for the switches and diodes. In addition, no auxiliary switch or extra magnetic element is employed in the proposed converter while the voltage stress of switches and diodes is rather low. These have led to simple structure, high density, low cost, and improved efficiency. Theoretical analysis and design considerations for the proposed converter are presented. Moreover, the experimental results of a 48 to 500 V laboratory prototype approve the effectiveness of the proposed topology.**

***Index Terms*—Coupled inductors, high step-up, interleaving technique, soft switching.**

I. Introduction

CURRENTLY, renewable power resources are getting remarkable attention due to their extensive availability and environmental issues like climate change [1]. In order to elevate the low output voltage of the renewable sources to the voltage level of dc bus, high step-up converters are required [1], [2].

In general, high step-up converters can be categorized into isolated and nonisolated topologies. In the isolated high step-up converters, desirable voltage conversion ratio is achieved by altering the transformer turns ratio [3], [4]. However, isolated topologies are voluminous and increase the system loss and cost. Therefore, when the electrical isolation is not necessary, the efficient solution is to utilize nonisolated converters. The most investigated nonisolated high step-up converters are those that employ coupled inductors to adjustably increase the voltage gain [2], [5]–[22]. The basic structure of this category of converters is the tapped inductor boost converter which can achieve high voltage gain while employing very low number of elements [5]. However, it suffers from two major drawbacks of pulsating input current, and sever voltage spikes across the semiconductors due to the leakage inductance of the coupled inductors. In order to reduce the input current ripple specially in high power applications, interleaving along with winding-cross-coupled inductors (WCCIs) techniques are utilized [10]–[22]. By using the interleaving technique, the elements current stress is reduced and the thermal distribution is improved [23]. In order to suppress the voltage spikes associated to the leakage inductance, in some interleaved WCCIs high step-up converters, passive clamp circuits are used [11]–[14]. However, they all suffer from hard switching condition at turn-OFF while using many passive elements.

Soft switching techniques are essential in high-frequency converters to reduce switching loss and electromagnetic interference [23]. The existing soft switching interleaved WCCIs high step-up converters mainly use active soft switching techniques such as zero voltage transition ([15], [16]), and active clamp circuits ([17]–[22]). In these techniques, the switching and capacitive turn-ON losses are diminished, but at the cost of using extra switches. Additional switches increase the converter complication, cost, and size. Some of these converters also have other disadvantages such as hard switching performance of the auxiliary switch and diodes which reduces the converter efficiency [16]. The interleaved WCCIs high step-up converters of [17]–[22] employ active clamp circuits and are capable of providing zero voltage switching condition for the switches. However, except for the topology presented in [22] which utilizes one active clamp circuit for two phases, the other converters require two auxiliary switches. Besides, in general, active clamp circuits do not provide soft switching at light loads.

Despite active soft switching techniques, passive lossless snubbers do not need any extra switch and hence, present a low-cost high-efficiency structure. This technique is applied to high step-up converters presented in [7]–[9]. However, these single-phase converters suffer from limited capacity of increasing the output power. Besides, the input currents of the converters presented in [8] and [9] are pulsating.

Developing a low-cost, highly efficient, and compact high step-up converter is extremely beneficial in renewable energy systems [19]. To meet these requirements, in the first step, by improving the basic structure of tapped inductor high step-up converter of [5], a novel soft switching coupled inductors-based single-phase high step-up converter with an advanced passive lossless snubber is introduced. This novel single-phase converter is shown in Fig. 1. The secondary winding of the tapped inductors, L_{a1} has two different functions in the proposed converter: it enhances the converter voltage gain and at the same time, it helps to provide soft switching condition for the converter elements.

Manuscript received March 19, 2020; revised July 4, 2020 and September 17, 2020; accepted October 10, 2020. Date of publication October 29, 2020; date of current version December 18, 2020. *(Corresponding author: Hosein Farzanehfard.)*

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Digital Object Identifier 10.1109/JESTIE.2020.3033542

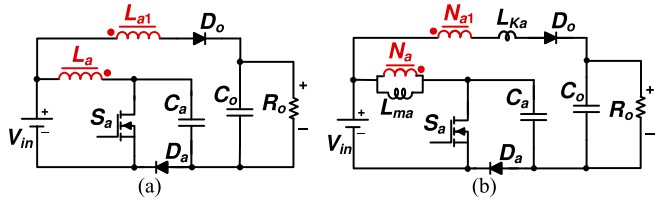

Fig. 1. (a) Proposed single-phase high step-up converter. (b) Equivalent circuit.

L_{ma} is the magnetizing inductance of the coupled inductors. The leakage inductance of the coupled inductors, L_{Ka} has three main roles in providing soft switching condition: it is the turn-ON snubber inductor for S_a, it discharges C_a and consequently helps to provide soft switching condition at turn-OFF for S_a, it also controls the current falling rate of D_o. Complete converter analysis is performed for the two-phase interleaved structure in the next section.

The proposed single-phase converter has many advantages such as simple structure with low number of elements and low cost, high voltage gain, high efficiency due to full soft switching operation, and alleviating the reverse recovery problem of D_o. In comparison with the single-phase high step-up converters with passive lossless snubbers presented in [7]–[9], the proposed converter uses the least number of auxiliary elements. In fact, the proposed converter uses only one extra diode comparing to the basic tapped inductor high step-up converter of [5] while in contrast, has soft switching feature. However, the basic converter of Fig. 1 suffers from pulsating current at the input similar to the tapped inductor high step-up converter of [5]. Therefore, in the second step, in order to overcome this shortcoming, increase the converter voltage gain, and have the benefits of interleaved structure, the basic single-phase converter is developed and by sharing common components and cross coupling the inductors, the proposed interleaved WCCIs soft switching high step-up converter is obtained as shown in Fig. 2. This converter is fully soft switched with low input current ripple while it utilizes low number of elements in comparison with the existing soft switching high step-up interleaved WCCIs converters. In the proposed converter, the coupled inductors have triple functions of elevating the voltage gain, performing soft switching, and smoothing the input current. This causes the magnetic cores to be efficiently occupied and thus, reduces the overall size and cost of the proposed converter and enhances the power density. The proposed converter is capable of attaining ten-fold voltage gain without any large coupled inductors turns ratios.

II. Operational Principles and Analysis

A. Proposed Interleaved WCCIs High Step-Up Converter

The proposed soft switching high step-up interleaved converter and its equivalent circuit are shown in Fig. 2. S_a and S_b denote the converter switches; C_a and C_b are the resonant capacitors; D_o, D_a, and D_b are the converter output and auxiliary diodes, respectively; C_o is the output capacitor; $V_{\rm in}$ and $V_{\rm out}$ represent the input and output voltages, respectively; and R_o is

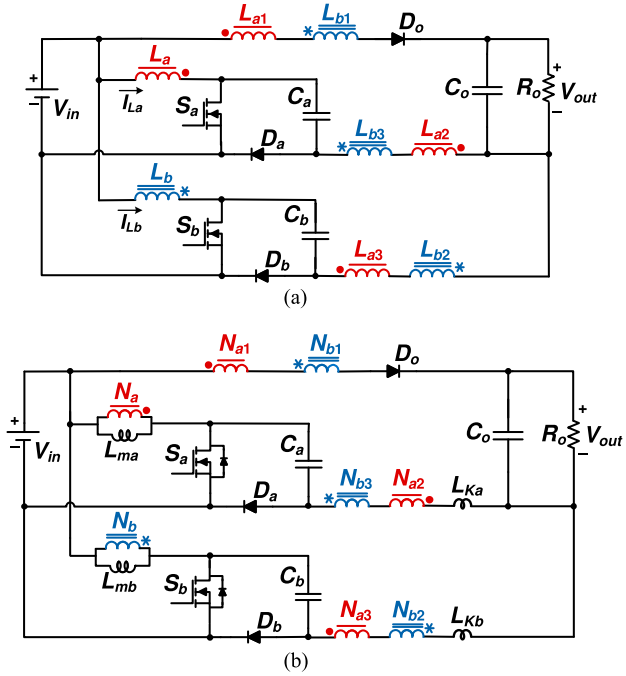

Fig. 2. (a) Proposed interleaved high step-up converter. (b) Equivalent circuit.

the load. The converter employs two coupled inductors with the same number of turns at the primary side. In one interleaved phase, the primary winding L_a with N_a turns is coupled to L_{a1} with N_{a1} turns, L_{a2} with N_{a2} turns in one phase, and L_{a3} with N_{a3} turns in the other phase. Similar coupling is provided in the other phase. D_a and D_b provide the return path of the energy, and also prevent discharging of C_a and C_b in S_a and S_b, respectively. L_{ma} and L_{mb} are the magnetizing inductances of the coupled inductors and L_{Ka} and L_{Kb} represent the equivalent leakage inductances which are shown on the secondary side. L_{a2}–L_{b3} and also L_{b2}–L_{a3} are connected in series at the high-voltage side to uplift the converter voltage gain. They also help to reduce the input current ripple and the converter switches voltage stress by implementing WCCIs technique. L_{Ka} and L_{Kb} play the role of the switches snubber inductors. The leakage inductances also discharge the converter resonant capacitors and help to provide zero voltage zero current switching (ZVZCS) condition at turn OFF for the converter switches. The input average current ($I_{\rm in}$) is distributed between three windings of L_a, L_b, and L_{a1}. In order to simplify the analysis and due to symmetry of interleaved structure, it is assumed that $N_a = N_b$, $N_{a1} = N_{a2} = N_{a3} = N_{b1} = N_{b2} = N_{b3} = N$, $N/N_a = N/N_b = n$, $C_a = C_b = C_r$, $L_{ma} = L_{mb} = L_m$, and $L_{Ka} = L_{Kb} = L_K$. The converter switches and diodes are selected identical and assumed to be ideal.

B. Steady-State Principles and Analysis

It is assumed that the converter operates at steady state and continuous conduction mode. The voltage gain is adjusted by changing the switching frequency $f_{\rm sw}$. The proposed converter provides ZCS turn-ON condition for the switches in both below and above resonant frequencies and operating at below-resonant frequencies leads to smaller resonant elements. Therefore, the

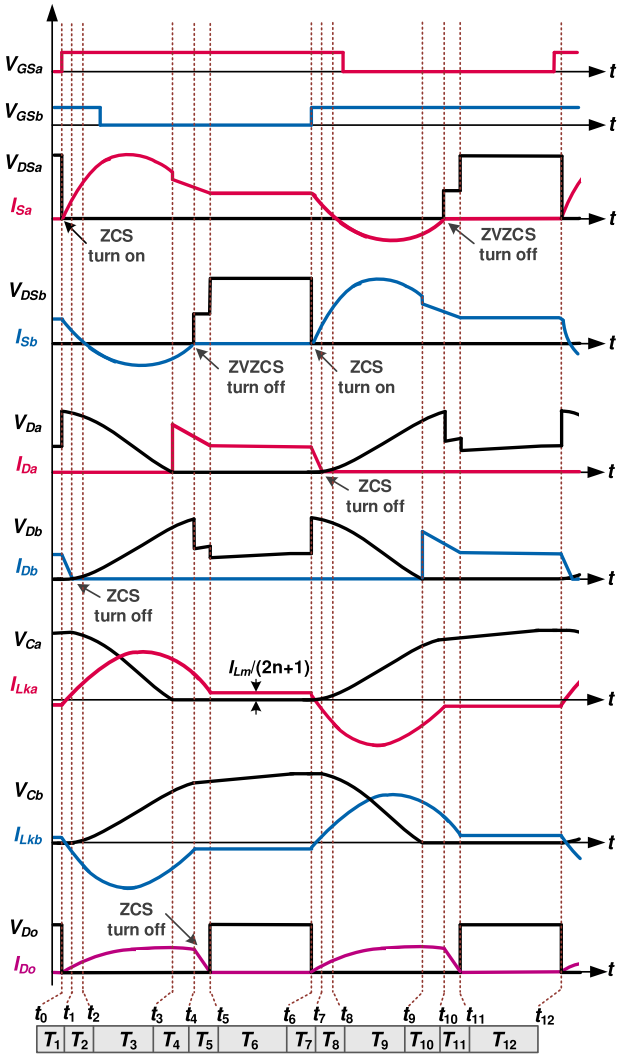

Fig. 3. Key waveforms of the proposed converter.

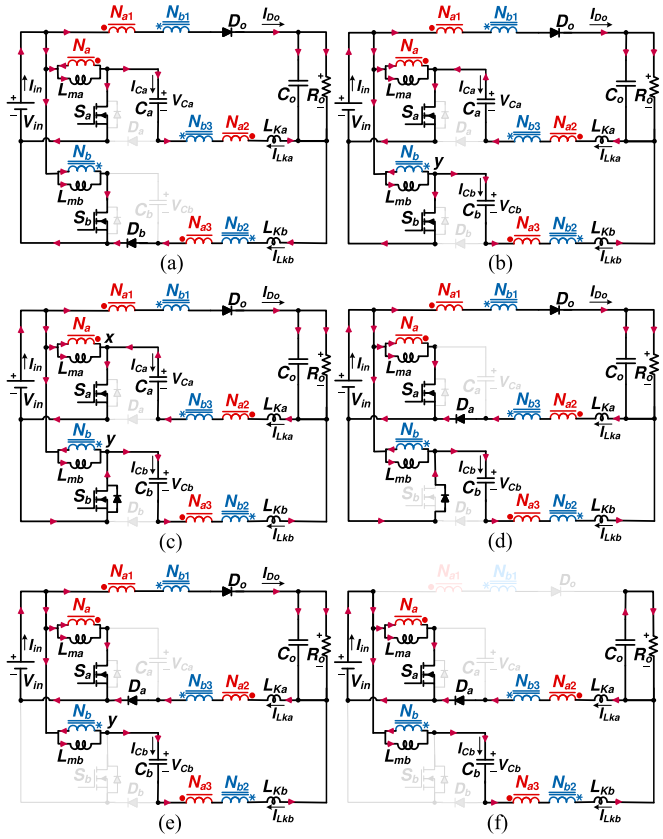

Fig. 4. Equivalent circuits of operating modes. (a) Mode 1. (b) Mode 2. (c) Mode 3. (d) Mode 4. (e) Mode 5. (f) Mode 6.

below-resonant operation is chosen for the proposed converter. In this region, if $f_{\rm sw}$ is selected far enough from f_r, the voltage gain curve would be quasi-linear which leads to weak dependency of the voltage gain on the load variations. Besides, in this region, the resonant peak current has an acceptable value [24], [25]. Therefore, below-resonant quasi-linear operation is selected for the proposed converter. Twelve modes of operation occur during one switching cycle and due to the symmetry of the interleaved structure, the first six modes in half a switching period are analyzed. Fig. 3 shows the key waveforms and Fig. 4 illustrates the equivalent circuits of the various operating modes.

Before t_0, S_b and D_b are ON and other semiconductors are OFF. $V_{\rm in}$ is charging L_{mb} and C_o is supplying the load. $V_{Cb}(t_0) = 0$ and $V_{Ca}(t_0)$ is obtained in Section III. T_1 to T_6 in Fig. 3 are the time transitions of modes 1 to 6, respectively.

Mode 1 [t_0–t_1] [Fig. 4(*a*)]: At t_0, S_a is turned ON at ZCS due to L_{Ka}. Consequently, a resonance occurs between C_a and L_{Ka}. D_o turns ON at t_0 as well and starts delivering energy to the output. In the other phase, V_{Cb} remains zero, while I_{Lkb} decreases linearly according to (1) because of the negative voltage across it. I_{Lkb} becomes zero at t_1 and thus, D_b turns OFF at ZCS, and this mode ends. The important equations of this mode are

$$I_{L_{Kb}}(t) = -\left(A_1/L_K\right)(t-t_0) + I_{L_{Kb}}(t_0) \tag{1}$$

$$V_{C_a}(t) = A_1 + B_1 \sin\left(\omega_r(t-t_0)\right) + C_1 \cos\left(\omega_r(t-t_0)\right) \tag{2}$$

$$I_{L_{Ka}}(t) = -I_{C_a}(t) = -C_r\left(dV_{C_a}/dt\right) \tag{3}$$

where

$$A_1 = V_{\rm out} - (2n+1)V_{\rm in},$$
$$B_1 = Z_r I_{\rm in}/(3(2n+1)), C_1 = V_{C_a}(t_0) - A_1 \tag{4}$$
$$\omega_r = 1/\sqrt{L_K C_r}, Z_r = \sqrt{L_r/C_r}. \tag{5}$$

Mode 2 [t_1–t_2] [Fig. 4(*b*)]: At the beginning of this mode, a new resonance begins between C_a, L_{Ka}, C_b, and L_{Kb} through which V_{Ca} starts to decrease, while V_{Cb}, I_{Lka}, and I_{Cb} start to increase. At t_2, I_{Cb} rises enough to force S_b antiparallel diode to conduct. The defining equations of this resonance are

$$V_{C_a}(t) = A_1 + B_2 \sin\left(\omega_r(t-t_1)\right) + C_2 \cos\left(\omega_r(t-t_1)\right) \tag{6}$$

$$V_{C_b}(t) = A_1\left[1 - \cos\left(\omega_r(t-t_1)\right)\right] \tag{7}$$

$$I_{L_{K_{a,b}}}(t) = -I_{C_{a,b}}(t) = -C_r\left(dV_{C_{a,b}}/dt\right) \tag{8}$$

where

$$B_2 = -Z_r I_{L_{Ka}}(t_1), \quad C_2 = V_{C_a}(t_1) - A_1. \tag{9}$$

Mode 3 [t_2–t_3] [Fig. 4(*c*)]: At t_2, S_b antiparallel diode starts conducting and thus, S_b can be turned OFF at ZVZCS during this mode. The resonance of the previous interval continues in this mode. At t_3, V_{Ca} becomes zero and D_a turns ON. The following equations are valid for this mode:

$$V_{C_a}(t) = A_1 + B_3 \sin(\omega_r(t-t_2)) + C_3 \cos(\omega_r(t-t_2)) \quad (10)$$

$$V_{C_b}(t) = A_1 + B'_3 \sin(\omega_r(t-t_2)) + C'_3 \cos(\omega_r(t-t_2)) \quad (11)$$

$$I_{L_{Ka,b}}(t) = -I_{C_{a,b}}(t) = -C_r\left(dV_{C_{a,b}}/dt\right) \quad (12)$$

$$T_3 = \left[\cos^{-1}\left(-A_1/\sqrt{B_3^2+C_3^2}\right) + \tan^{-1}(B_3/C_3)\right]/\omega_r \quad (13)$$

where

$$B_3 = -Z_r I_{L_{Ka}}(t_2), \quad C_3 = V_{C_a}(t_2) - A_1 \quad (14)$$

$$B'_3 = -Z_r I_{L_{Kb}}(t_2), \quad C'_3 = V_{C_b}(t_3) - A_1. \quad (15)$$

Mode 4 [t_3–t_4] [Fig. 4(*d*)]: At the start of this mode, a new resonance occurs between C_b and L_{Kb}. Through this resonance, V_{Cb} increases while I_{Cb} decreases. Also, at t_3, I_{L1} and I_{Lka} start to decrease linearly due to the negative voltage induced on L_{Ka}. At the end of this mode, $I_{Cb} = I_x$ and hence, S_b antiparallel diode turns OFF at ZCS. For this mode, the below equations are valid:

$$I_{L_{Ka}}(t) = -(A_1/L_K)(t-t_3) + I_{L_{Ka}}(t_3) \quad (16)$$

$$V_{C_b}(t) = A_1 + B'_4 \sin(\omega_r(t-t_3)) + C'_4 \cos(\omega_r(t-t_3)) \quad (17)$$

$$I_{L_{Kb}}(t) = -I_{C_b}(t) = -C_r(dV_{C_b}/dt) \quad (18)$$

$$T_4 = \left[\cos^{-1}\left(B_1/\sqrt{B'^2_4+C'^2_4}\right) + \tan^{-1}(-C'_4/B'_4)\right]/\omega_r \quad (19)$$

where

$$B'_4 = -Z_r I_{L_{Kb}}(t_3), \quad C'_4 = V_{C_b}(t_3) - A_1. \quad (20)$$

Mode 5 [t_4–t_5] [Fig. 4(*e*)]: During this transition, I_{L1} and I_{Lka} continue to decrease linearly with the same slope as the previous mode. By applying KCL principle to node *y*, I_{Lkb} is obtained as described by (21). Thus, in this mode, V_{Cb} begins to increase linearly. At t_5, I_{L1} becomes zero and hence, D_o turns OFF at ZCS. Defining equations of this transition are

$$I_{L_{Kb}}(t) = -I_{C_b}(t) = I_{\rm in}/(3(2n+1)) \quad (21)$$

$$V_{C_b}(t) = [I_{\rm in}/(3(2n+1)C_r)](t-t_4) + V_{C_b}(t_4) \quad (22)$$

$$I_{L_{Ka}}(t) = -(A_1/L_K)(t-t_4) + I_{L_{Ka}}(t_4). \quad (23)$$

Mode 6 [t_5–t_6] [Fig. 4(*f*)]: In this interval, S_a and D_a are conducting while all other semiconductors are OFF. V_{Cb} continues to increase linearly with the previous slope. $V_{\rm in}$, is charging L_{ma}, while L_{mb} is discharging and C_o is supplying the load. At t_6, S_b turns ON at ZCS and the next half a switching cycle begins. For this mode, the following equations can be written:

$$I_{L_{Ka}} = -I_{L_{Kb}} = I_{in}/(3(2n+1)) \quad (24)$$

$$T_6 = 0.5T_{\rm sw} - (T_1+T_2+T_3+T_4+T_5). \quad (25)$$

III. Steady-State Analysis

In order to simplify the mathematical analysis, the short time transitions of T_1, T_2, and T_5 are ignored. Furthermore, since the converter has symmetrical operation for two phases, the voltages and currents of phase *b* are exactly the same as those of phase *a* with 180° phase shift and thus, $V_{Ca}(t_{0+m}) = V_{Cb}(t_{6+m})$, $I_{Lka}(t_{0+m}) = I_{Lkb}(t_{6+m})$ where $0 \le m \le 6$.

A. Voltage Gain Calculation

The average current of the output diode is equal to the load current $I_{\rm out}$ at the steady-state condition.

$$I_{\rm out} = V_{\rm out}/R_o = (2/T_{\rm sw})\int_{t_0}^{t_6} I_{Do}(t).dt. \quad (26)$$

Since I_{Do} is equal to the summation of I_{Lka} and I_{Lkb} during modes 1 to 5 and by neglecting the short time transitions of T_1, T_2, and T_5, (26) can be rewritten as

$$I_{\rm out} = 2f_{\rm sw}\int_{t_2}^{t_4}(I_{L_{Ka}} + I_{L_{Kb}}).dt. \quad (27)$$

Exact equations of I_{Lka} and I_{Lkb} in modes 3 and 4 are given in (12), (16), and (18). Also, the exact relations for obtaining T_3 and T_4 are written in (13) and (19), respectively. However, to simplify the calculations, some minor approximations must be made. In Fig. 3, by considering I_{Lkb} waveform in T_3 and T_4

$$T_3 + T_4 \simeq T_r/2 \quad (28)$$

where $T_r = 2\pi/\omega_r$ is the resonance period of C_r and L_K. Thus, the time interval of T_6 is approximated as

$$T_6 \simeq (T_{\rm sw} - T_r)/2. \quad (29)$$

To obtain I_{Lka} and I_{Lkb} during modes 3 and 4, first $V_{Ca}(t_0) = V_{Cb}(t_6)$ should be determined. To analytically calculate $V_{Cb}(t_6)$, the following procedure is performed: from Fig. 4(c) and (d), by neglecting T_1 and T_2 and supposing that the resonance between C_b and L_{Kb} starts at t_2, I_{Lkb} in modes 3 and 4 is approximated as

$$I_{L_{Kb}}(t) = [((2n+1)V_{\rm in} - V_{\rm out})/Z_r]\sin(\omega_r(t-t_2)), [t_2, t_4]. \quad (30)$$

Considering (30), V_{Cb} can be approximated as

$$V_{C_b}(t) = ((2n+1)V_{in} - V_{out})\cos(\omega_r(t-t_2)), [t_2, t_4]. \quad (31)$$

Using (31), after half a resonance period, V_{Cb} becomes

$$V_{C_b}(t_4) = 2(V_{\rm out} - (2n+1)V_{\rm in}). \quad (32)$$

Using (22) and by neglecting the short time transition of T_5 and substituting T_6 from (29), $V_{Cb}(t_6)$ is calculated as

$$V_{C_b}(t_6) = 2(V_{\rm out} - (2n+1)V_{\rm in}) + (I_{\rm in}(T_{\rm sw} - T_r))/(6C_r(2n+1)). \quad (33)$$

By applying KVL principle to the loop consisting of S_b, C_b, N_{a3}, N_{b2}, L_{Kb}, L_{Ka}, N_{a2}, N_{b3}, C_a, and S_a in Fig. 4(*c*), I_{Lka} is

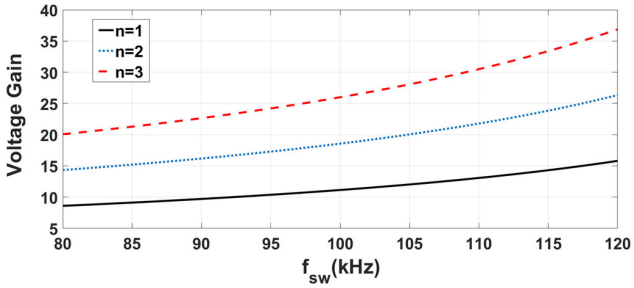

Fig. 5. Voltage gain of the proposed converter versus switching frequency ($f_{\rm sw}$) for different values of turns ratio (n).

obtained as

$$I_{L_{Ka}}(t) = \{[V_{Ca}(t_2) + (2n+1)V_{\rm in} - V_{\rm out}]/Z_r\} \times \sin(\omega_r(t-t_2)),\ \ [t_2, t_3]. \quad (34)$$

Since T_1 and T_2 are very short, it can be concluded that $V_{Ca}(t_2) \approx V_{Ca}(t_0)$ which is equal to $V_{Cb}(t_6)$. Therefore, from (33) and (34):

$$I_{L_{Ka}}(t) = \{[V_{\rm out} - (2n+1)V_{\rm in} + (I_{\rm in}(T_{\rm sw} - T_r))/(6C_r(2n+1))]/Z_r\} \times \sin(\omega_r(t-t_2)),\ \ [t_2, t_3]. \quad (35)$$

I_{Lka} in mode 4 is given in (16). However, since T_4 is a small transition and I_{Lka} in (16) starts with initial value of $I_{Lka}(t_3)$ which is obtained from (35), the linear equation of (16) can be approximated by a sinusoidal waveform which is the continuation of (35). In other words, in both modes 3 and 4, I_{Lka} can be shown by the sinusoidal waveform of (35). Therefore, by substituting (30) and (35) in (27), and considering $T_{sw} = 1/f_{\rm sw}$ and $T_r = 1/f_r$, I_{out} is obtained as follows:

$$I_{\rm out} = [2I_{\rm in}(1 - f_{\rm sw}/f_r)]/(3(2n+1)). \quad (36)$$

Therefore, by substituting (36) in (26), the final expression of the converter voltage gain is obtained as (37)

$$V_{\rm out}/V_{\rm in} = [3(2n+1)]/[2(1 - f_{\rm sw}/f_r)]. \quad (37)$$

The above relation confirms that the proposed converter can achieve a high voltage gain even at $n = 1$ and higher voltage gains can be achieved by increasing the turns ratio. The converter voltage gain as a function of switching frequency is plotted for various turns ratios in Fig. 5. As can be observed, for $n = 1$, when the switching frequency reaches 100 kHz, a voltage gain of more than 10 is achieved.

B. Voltage and Current Stress Analysis

By applying KVL principle to the loop composed of N_b, S_b, and V_{in} in Fig. 4(*f*), the voltage stresses of the semiconductors are obtained as

$$V_{S_{a,b(\max)}} = [2V_{\rm out}/(2n+1)][1 - (2/3)(1 - f_{\rm sw}/f_r)] \quad (38)$$

$$2V_{D_{o(\max)}} = V_{D_{a,b(\max)}} = 2V_{\rm out}[1 - (2/3)(1 - (f_{\rm sw}/f_r))]. \quad (39)$$

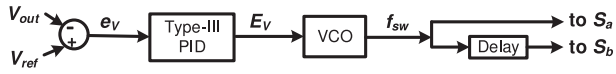

Fig. 6. Block diagram of the variable frequency control loop.

Equation (38) shows that by increasing n, the voltage stress of the switches decreases and hence, low-voltage rated power MOSFETs can be chosen for the switches. The current stress of the switches is influenced by the peak current of the leakage inductance in mode 3 and can be extracted by applying KCL principle to node x as follows:

$$I_{S_{a,b(\max)}} = (I_{\rm in(max)}/3) + (2n+1)\omega_r C_r \sqrt{B_3^2 + C_3^2}. \quad (40)$$

Likewise, the converter diodes current stress are obtained from (12) as

$$I_{D_{o(\max)}} = I_{\rm in(max)}/(3(2n+1)) \quad (41)$$

$$I_{D_{a,b(\max)}} = \omega_r C_r \sqrt{B_3^2 + C_3^2 - A_1^2}. \quad (42)$$

IV. Design Procedure

The converter is designed to convert 40–50 V input voltage to 500 V output voltage at 250 W nominal output power. From (37), it can be observed that by increasing n, the converter voltage gain increases. Nevertheless, for simplicity and avoiding voluminous windings, n is selected 1 in the prototype converter. Also, the nominal switching frequency, $f_{\rm sw(nom)}$ is considered as 100 kHz. In order to guarantee that the converter operates in the quasi-linear area of the voltage gain curve, f_r is selected about $1.5 \times f_{\rm sw(nom)}$. Therefore, f_r is selected 150 kHz.

The proposed converter uses very low number of elements and thus, two same switches, three diodes, the filter inductors and capacitor, and the resonant capacitor must be chosen.

A. Selection of the Semiconductor Elements

Using (38)–(42), the semiconductors voltage and current stresses are attained. Two IPP410N30N are used as the converter switches, one MUR460 is selected for the output diode, and two UF5407 are used as the auxiliary diodes.

B. Selection of the Passive Elements

As shown in Fig. 3, the summation of the conducting intervals of the switch and its antiparallel diode, t_S is about $(T_{\rm sw} + T_r)/2$. Consequently, for the prototype converter $t_S \approx 0.8$ μs. The magnetizing inductance is selected in such a way that its current variation would be 20% $\times$ $I_{\rm in}$ to reduce the coupled inductors size. Considering $V_{\rm in} = 50$ V and $t_S = 8$ μs, L_m is calculated as 400 μH. The output capacitor is designed according to the tolerable variations of the output voltage like that of a boost converter, i.e., 0.05 $\times$ $V_{\rm out}$ and thus, C_o is obtained as 33 μF.

As a turn-ON snubber, the minimum value of L_K is calculated from [26]. Even with a good coupling, the measured value of L_K provides enough inductance for the snubber value. L_K value is measured as 75 μH and by knowing this value and considering $\omega_r (= 2\pi f_r)$, C_r is calculated using (5) equal to 15 nF. Table I

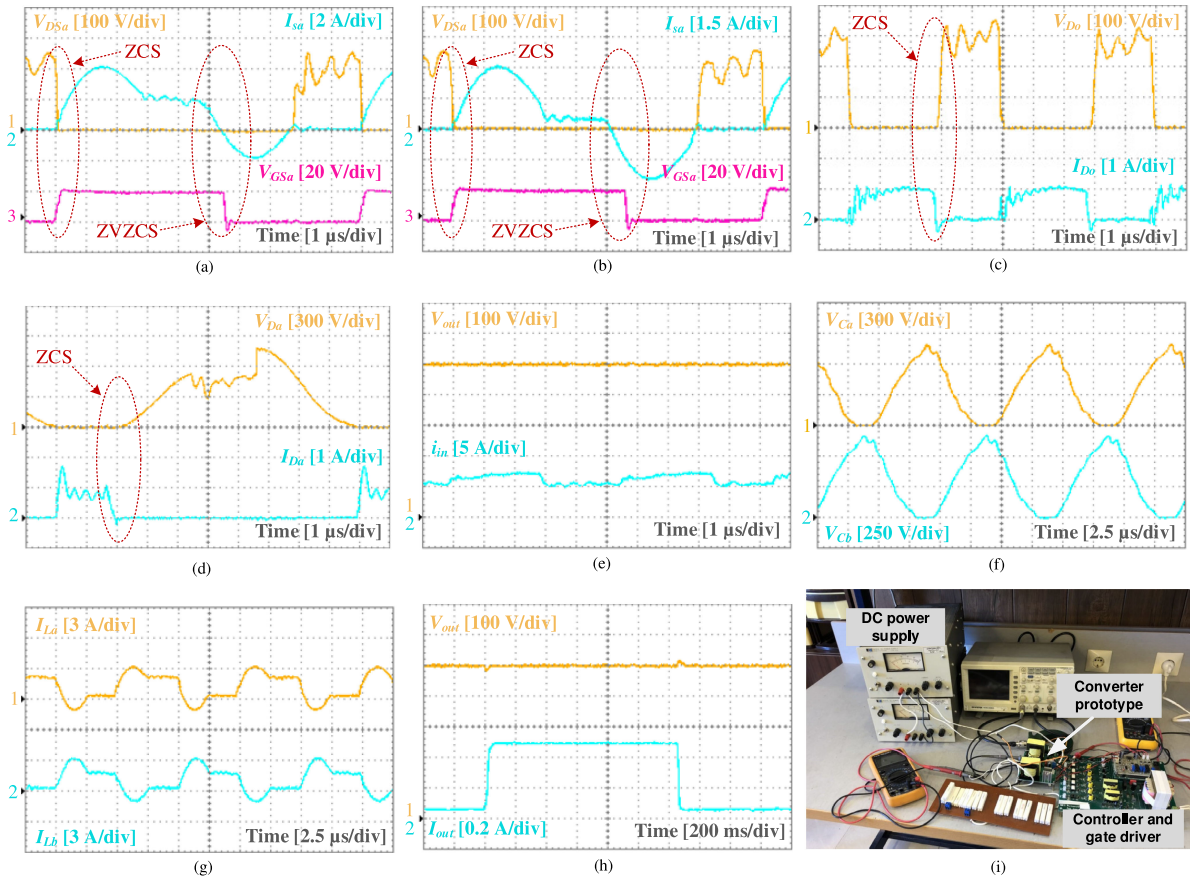

Fig. 7. Experimental voltage and current waveforms and the exponential setup. (a) S_a at full load. (b) S_a at 10% load. (c) D_o at full load. (d) D_a at full load. (e) $V_{\rm out}$ and $i_{\rm in}$ at full load. (f) C_a and C_b voltages at full load. (g) L_a and L_b currents at full load. (h) Dynamic response due to 10% to 100% step load change. (i) Photo of the experimental setup.

TABLE I
SPECIFICATIONS OF THE PROPOSED CONVERTER PROTOTYPE

Parameter	Symbol	Specification
Input voltage	V_{in}	40 V-50 V
Output voltage	V_{out}	500 V
Output power	P_{out}	250 W
Switching frequency range	f_{sw}	85 kHz-110 kHz
Switches	S_a, S_b	IPP410N30N
Output diode	D_o	MUR460
Auxiliary diodes	D_a, D_b	UF5407
Output capacitor	C_o	33 µF
Magnetizing inductances	L_{ma}, L_{mb}	400 µH
Equivalent leakage inductances	L_{Ka}, L_{Kb}	75 µH
Resonant capacitors	C_a, C_b	15 nF
Turns ratio	n	1

TABLE II
LOSS BREAKDOWN TABLE OF THE PROPOSED CONVERTER

Type of loss	Loss value (W)
S_a and S_b switching loss	zero due to soft switching
S_a and S_b capacitive turn on loss	1.12
S_a and S_b conduction loss	0.42
D_o conduction loss	0.5
D_a and D_b conduction loss	0.92
Core loss	1.82
Copper loss	2.9
Total theoretical loss	7.68
Total experimental loss	9.18

represents the selected parameters and elements of the prototype converter.

The duty cycle must be selected between 0.5 and $(0.5+t_{2-4}/T_{\rm sw})$ so that ZVZCS turn-OFF can be achieved for the switches. However, D is fixed at about 0.5 to have low input current ripple in the proposed interleaved structure.

V. CONTROL STRATEGY OF THE PROPOSED CONVERTER

For the proposed converter, a simple and straightforward variable frequency control technique is utilized. This method is shown in Fig. 6. The output voltage is compared to a reference voltage in a comparator to produce the error signal e_V. The error signal is amplified in a conventional type III proportional integral derivative (PID) controller. Then, the PID controller output, E_V is applied to a voltage-controlled oscillator (VCO) in order to generate the gate signals with appropriate frequency proportional to E_V. The delay block in Fig. 6 provides required 180° phase shift between the switches gate signals of two interleaved phases.

TABLE III
CONVERTER PERFORMANCE COMPARISON

Feature		[12] and [13]	[14]	[17]	[18]	Proposed converter
Soft switching at turn on		ZCS	ZCS	ZVS	ZVS	ZCS
Soft switching at turn off		hard-switched	hard-switched	ZVS	ZVS	ZVZCS
Switches		2	2	4	4	2
Diodes		4	5	6	4	3
Magnetic cores		2	2	2	2	2
Capacitors		4	4	9	7	3
Voltage gain		$\frac{2(n+2)}{1-D}$	$\frac{3n+1}{1-D}$	$\frac{2(n+1)}{1-D}\frac{1}{1+\left(8n^2L_K f_{sw}/R_o\right)/(1-D)^2}$	$\frac{4(2n+1)}{(1-D)+\sqrt{(1-D)^2+6k}}$, $k=8n^2(2n+1)f_{sw}L_K/\left((n+1)R_o\right)$	$\frac{3(2n+1)}{2\left(1-f_{sw}/f_r\right)}$
Main switches voltage stress		$V_{out}/\left(2(n+2)\right)$	$V_{out}/(3n+1)$	$V_{out}/\left(2(n+1)\right)$	$V_{out}/\left(2(2n+1)\right)$	$1.6V_{out}/(2n+1)$
Main diodes voltage stress		$(n+1)V_{out}/(n+2)$	$2nV_{out}/(3n+1)$	$(2n+1)V_{out}/(2(n+1))$	$V_{out}/2$	$0.8V_{out}$
Effect of the leakage inductance on voltage gain		Not reported	Negative	Negative	Negative	Positive
Converter spec.	V_{in}, V_{out}	20 V, 400 V	40V, 400 V	15~30 V, 270 V	30 V, 600 V	40~50 V, 500 V
	$P_{out(\text{nom})}$	320 W ([12]) 280 W ([13])	400 W	1000 W	1000 W	250 W
	Reported efficiency	94.9 % ([12]) 95.01 %([13])	97.3 %	97.2 %	97.5 %	96.5 %
Control method		PWM	PWM	PWM	PWM	Frequency controlled

VI. EXPERIMENTAL RESULTS

A laboratory prototype of the proposed converter is implemented considering the design procedure of Section III. Fig. 7 displays the converter prototype and the experimental waveforms. Fig. 7(a) shows the voltage and current waveforms of S_a at the nominal load. As this figure shows, the switch turns ON at ZCS. Also, the switch gate signal is removed after the anti-parallel diode turn-ON to provide ZVZCS turn-OFF for the switch. Fig. 7(b) displays the switch waveforms at 10% of nominal load confirming the switch ZCS turn-ON and ZVZCS turn OFF. Also, it is evident that the switch voltage stress is about half of the output voltage. Figs. 7(c) and (d) demonstrate the voltage and current waveforms of D_o and D_a at full load, respectively. As can be observed, the diodes turn-OFF at ZCS and thus, their reverse recovery problem is relieved. Fig. 7(e) shows the converter output voltage and input current. The interleaved operation of the converter which leads to identical waveforms with 180° phase shift is clearly evident from Figs. 7(f) and (g). Fast response and very low overshoot is observed from Fig. 7(h) which shows the converter dynamic response due to load transient from 100% to 10% and vice versa. The experimental setup is shown in Fig. 7(i). Fig. 8 exhibits the efficiency of the prototype converter versus the output power. The converter maximum efficiency of 96.5% is achieved at the nominal output power. The converter detailed loss breakdown analysis at full load is presented in Table II.

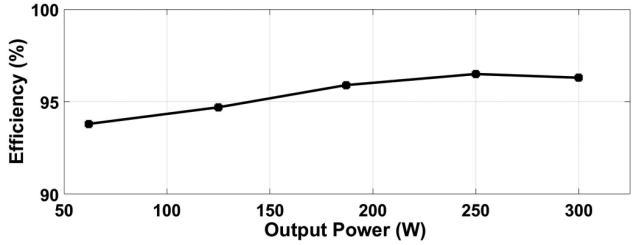

Fig. 8. Efficiency of the proposed converter at different output powers.

VII. PERFORMANCE COMPARISON

Features of the proposed converter are compared to those of some recent and prominent counterparts and the results are presented in Table III. All the topologies included in this table are interleaved high step-up converters with WCCIs. As Table III shows, the proposed converter can provide high-voltage gain as well as full soft switching feature for all the semiconductors while using the least number of switches and diodes. Unlike the converters of [14], [17], and [18], the leakage inductance has a positive effect on the proposed converter voltage gain. In Table III, the proposed converter semiconductors voltage stress at the worst case of $f_{\text{sw}(\max)}$ is presented. In the proposed converter, similar to other converters with resonant nature, the switch voltage stress is higher than the PWM counterparts. Instead, the proposed converter is capable of providing full soft switching feature without using any extra switches and with low number of auxiliary elements. This is while in [12]–[14], full soft switching feature is not provided and in [17] and [18], full soft switching condition is achieved but at the cost of using two extra switches with many extra passive elements.

VIII. CONCLUSION

In this article, first a single-phase high step-up soft switching converter was introduced and then its interleaved topology was

developed. This compact topology has higher voltage gain with smooth input current, while providing soft switching condition for all semiconductor devices and achieving high efficiency. The presented theoretical analysis was validated by a 48–500 V prototype of the proposed converter operating at 250 W. The experimental results show that the converter switches operate at ZCS turn-ON and ZVZCS turn-OFF even at very light loads. Besides, their voltage stress is half of the output voltage. The experimental results also show that the converter diodes turn-OFF at ZCS and hence, their reverse recovery problem is relived. The dynamic response due to the step load confirms the fast and accurate response of the proposed converter.

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